REMARKS

Claims 1-20 are pending, with Claims 1 and 6 being independent. Reconsideration and allowance of the above-referenced application are respectfully requested.

Rejections Under 35 U.S.C. §103(a)

Claims 1 and 6 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 6, 119,016 issued to Matusevich (hereinafter "Matusevich") in view of U.S. Patent Application US 2002/0051509 A1 by Linder et al. (hereinafter "Linder").

Claims 3-4, 8, 11-12, and 16 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Matusevich in view of Linder and further in view of U.S. Patent No. 5,062,124 issued to Hayashi et al. (hereinafter "Hayashi").

Claims 2 and 7 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Matusevich in view of Linder and further in view of Hayashi, and further in view of U.S. Patent No. 6,791,987 issued to Eng et al. (hereinafter "Eng"). These contentions are respectfully traversed. These contentions are respectfully traversed.

The Subject Matter as Claimed

The subject matter as defined in claims 1 and 6 is a system and method for transmitting data from a source module to a terminating module over a network comprising a plurality of modules, in which each of the modules in the network operate with an independent clock. The terminating module is synchronized to the clock of the source module using an accumulated phase difference that is transmitted over the network to the terminating module. The accumulated phase difference is the difference between the input and output of each of the modules through which data is transmitted. The terminating module receives all of the accumulated phase differences and uses them to lock an output clock with an input clock of the source module.

Further, the claimed subject matter does not require synchronizing the clocks of each module in the network or synchronizing timing signals generated by each clock in the network.

The Prior Art

The Examiner is relying on the combination of Matusevich with Linder to reject the independent claims. Accordingly, the response is focused on these two prior art documents.

Matusevich

Matusevich is directed to a technique for synchronizing the timing signals of base stations in a wireless telecommunications network (see column 1, lines 6 to 10). It discloses a network that includes a plurality of base stations. The base stations each have a reference timing signal of the same frequency (column 5 lines 1 to 3) from which a timing signal is generated (column 5 lines 4 to 6). The timing signal of each base station is synchronized with the timing signal of every other base station.

This synchronization is achieved using a phase locked loop (PLL) 601-i which phase aligns the reference timing signal to a feedback signal to create the timing signal (see column 5 lines 47 to 49). The phase locked loop has as its input the reference timing signal, which is always of the same frequency, and the signal from a unanimity gate. The unanimity gate 603-i has as its input the output of the phase locked loop as well the timing signals from other base stations in the network. Using this arrangement of a phase locked loop having an input both from a reference timing signal and from timing signals from nearby base stations, it is possible to produce a timing signal that is synchronized to the timing signals of all other base stations in the network.

This is distinguishable from the claimed subject matter because the aim of Matusevich is to produce synchronization of all the base stations in the network. There is no transmission of phase differences between base stations, let alone transmission of an accumulated phase difference across the network.

Lindner

Lindner is directed to a phase locked loop that includes a phase detector that provides, as an output, a current pulse whose duration is the measure of a phase difference between an input signal and an output signal. This output is coupled to a downstream loop filter, which is, in turn, connected to the oscillator. The problem solved by the invention of Lindner is that of

undesirable jitter (paragraph 11). The use of a loop filter provides a proportional current to the oscillator rather than a pulsed signal. This means that when the phase detector detects a phase difference, requiring a temporary change of frequency of the oscillator, the change of frequency is smoothed out over an entire clock cycle, thus reducing jitter (see paragraph 11).

Lindner does not disclose transmitting phase differences between modules in a network. It only discloses a phase locked loop.

Combination of Matusevich with Lindner

If Matusevich were modified using the teaching of Lindner, it would be by replacing the phase-locked loop 601-i in Matusevich with the phase-locked loop taught by Lindner. This modification would provide Matusevich with a timing signal that suffers from less jitter. It would not, however, result in a system as claimed in claims 1 and 6 of the present application.

For example, neither Matusevich nor Lindner ever transmits as an output a phase difference between an input clock and an output clock of a network module. In both Matusevich and Lindner, the teaching is of using a phase-locked loop to synchronies the input and output signals from device. By contrast, the claimed subject matter does not use a phase-locked loop to synchronies inputs and outputs. The inputs and outputs of each module are not synchronized. In the claimed subject matter, a phase difference is calculated and the phase difference transmitted to a terminating base station. There is no hint or suggestion of this in the cited prior art.

Furthermore, it is not clear that the teaching of Matusevich and Lindner could be, (let alone would be) combined in any other manner than replacing the phase-locked loop of Matusevich with the phase-locked loop of Lindner. The Examiner has simply said that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Matusevich using the features taught by Lindner to provide outputs that are all phase-locked to each, other but which are not synchronized to the inputs, and means for determining the accumulated phase difference between the input clock and output clock of each module. It is not clear how he has arrived at this conclusion. As stated above, the purpose of Lindner and the purpose of Matusevich is to provide synchronization between input and output signals.

Therefore, the proposed Hayashi-Eng combination does not teach or suggest each and every limitation of claims 1 and 6, and claims 1 and 6 should be in condition for allowance.

Further, all the pending dependent claims are allowable by virtue of their dependence from claims 1 or 6.

Thus, all the pending claims are allowable for at least the reasons provided above.

The foregoing comments made with respect to the positions taken by the Examiner are not to be construed as acquiescence with other positions of the Examiner that have not been explicitly contested. Accordingly, the above arguments for patentability of a claim should not be construed as implying that there are not other valid reasons for patentability of that claim or other claims.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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/Cheng C. Ko/
Cheng C. Ko
Reg. No. 54,227

Fish & Richardson P.C.
PTO Customer No. 20985
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

JWK/jhg
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